

CLAIMS

What is claimed is:

1 1. A method for fabricating an etched grooved GaN-based permeable-base
2 transistor device, comprising:

3 opening a window for helium implantation on a hydride vapor phase epitaxy
4 (HVPE) grown n^+ GaN quasi-substrate layer, using optical lithography;
5 implanting helium on the n^+ GaN quasi-substrate layer over the window for helium
6 implantation, so as to provide an insulating layer for contact pads of the
7 device;

8 opening a window for collector fingers using E-beam lithography;
9 depositing an ohmic metallization layer over the window for the collector fingers;
10 lifting-off ohmic metallization, thereby forming the collector fingers;
11 opening a window for a self-aligned base recess using optical lithography; and
12 etching to recess a base layer to an n^- GaN quasi-substrate layer grown on the n^+
13 GaN quasi-substrate layer, wherein the etching is performed with a ramp
14 down in chuck bias voltage.

1 2. The method of claim 1 further comprising:
2 opening a window for a collector contact pad, using optical lithography;
3 depositing a high quality silicon nitride layer over the window for a collector
4 contact pad; and
5 lifting-off or wet chemical etching the high quality silicon nitride layer, thereby
6 forming a silicon nitride collector contact pad.

1 3. The method of claim 2 wherein the high quality silicon nitride layer is about
2 1000-2000Å thick, and is deposited over the window for helium implantation via plasma
3 enhanced chemical vapor deposition (PECVD).

1 4. The method of claim 2 further comprising:
2 opening a window for Ti metallization of the collector contact pad using optical
3 lithography;

4 depositing Ti over the window for Ti metallization of the collector contact pad; and
5 lifting-off Ti metallization, thereby forming a Ti collector contact pad.

1 5. The method of claim 4 further comprising:
2 opening a window for a second Ti metallization of the collector contact pad using
3 optical lithography;
4 depositing Ti over the window for the second Ti metallization of the collector
5 contact pad; and
6 lifting-off second Ti metallization, thereby forming a Ti cap over the collector
7 contact pad.

1 6. The method of claim 2 wherein depositing Ti over the window for Ti
2 metallization of the collector contact pad includes depositing Ti/Au at thicknesses of about
3 500Å/1000Å, respectively, using e-beam evaporation.

1 7. The method of claim 1 wherein the ramp down in chuck bias voltage is
2 about -200 VDC or more, the method further comprising:
3 depositing conformal silicon nitride for passivation of the recessed base layer;
4 directionally etching to remove silicon nitride on planes parallel to the n^+ GaN
5 quasi-substrate layer;
6 depositing a base metallization layer; and
7 lifting-off base metallization, thereby forming a base contact pad.

1 8. The method of claim 7 wherein an anneal is performed post-base
2 metallization so as to provide the base contact pad with low reverse current leakage and
3 low contact resistance.

1 9. The method of claim 1 further comprising:
2 opening an emitter etch/contact window using optical lithography;
3 etching an emitter recess to the n^+ GaN quasi-substrate layer;
4 depositing an emitter ohmic metallization layer over the etched emitter recess; and
5 lifting-off emitter ohmic metallization, thereby forming an emitter contact pad.

1 10. The method of claim 1 wherein the emitter ohmic metallization layer
2 includes at least one of titanium, aluminum, nickel, and gold.

1 11. The method of claim 1 further comprising:
2 opening a window for RF test pad metallization using optical lithography;
3 depositing an RF test pad metallization layer; and
4 lifting-off RF test pad metallization, thereby providing RF test pads.

1 12. The method of claim 1 wherein the helium implantation is achieved with an
2 implant depth of about 2 μm .

1 13. The method of claim 1 wherein the ohmic metallization layer over the
2 window for the collector fingers is Ti/Ni with thicknesses of 100Å and 400Å, respectively.

1 14. The method of claim 1 wherein the device has a plurality of collector
2 fingers about 0.2 μm wide and having a finger pitch between 1:1 and 1:3.

1 15. An etched grooved GaN-based permeable-base transistor device,
2 comprising:

3 a GaN emitter region having a thickness of about 6 to 10 μm , and grown on (0001)
4 sapphire using hydride vapor-phase epitaxy (HVPE) and He implantation
5 under base and collector contact pads at an implant angle of about 7°;

6 a GaN base region having a thickness of about 1 to 2 μm , and grown on the GaN
7 emitter region using molecular beam epitaxy (MBE); and

8 a GaN collector region having a thickness of about 0.1 to 0.3 μm , and a plurality of
9 collector fingers having finger sidewall angles of about 80° to 85° for 1:1
10 and 1:3 finger spacing, wherein the collector region is grown on the GaN
11 base region using MBE.

1 16. The device of claim 1 wherein the device has ten or more collector fingers
2 each about 0.2 μm wide.

1 17. The device of claim 1 wherein spacing between each collector finger is
2 smaller than 1 μm .

1 18. The device of claim 1 wherein the each collector finger has two adjacent
2 base contacts, the base contacts having a width substantially equivalent to the gate length
3 of the device.

1 19. An etched grooved GaN-based permeable-base transistor device,
2 comprising:

3 a GaN emitter region grown using hydride vapor-phase epitaxy (HVPE);

4 a GaN base region grown on the GaN emitter region using molecular beam epitaxy
5 (MBE); and

6 a GaN collector region grown on the GaN base region using MBE, and having a
7 collector pad region and a plurality of collector fingers, wherein the
8 collector fingers have a first height in the collector pad region and a second
9 height out of the collector pad region, with the first and second heights
10 configured so as to prevent disconnect between the collector fingers and the
11 collector pad region.

1 20. The device of claim 19 wherein the device has ten or more collector fingers
2 each about 0.2 μm wide.

1 21. A method for fabricating an etched grooved GaN-based permeable-base
2 transistor device, comprising:

3 opening a window for a base recess; and

4 etching to recess a base layer to an n^- GaN quasi-substrate layer grown on the n^+
5 GaN quasi-substrate layer, wherein the etching is performed with a ramp
6 down in chuck bias voltage.